AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning at page 3, line 21 as follows:

A first aspect of the present invention is providing a semiconductor memory device ~~having a gate electrode and a diffusion layer, comprising a plurality of memory cells each of which including the gate electrode and the diffusion layers; a first contact layer connected to one of the diffusion layer of the memory cell; a second contact layer connected to the first contact layer; a bit line connected to the second contact layer; and a conductive layer connected to at least two of the diffusion layers that are other than the diffusion layer connected to the first contact layer, at least two of the diffusion layers being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being the same as a height of the first contact layer~~, a first memory cell having a first gate electrode, a first diffusion layer and a second diffusion layer, the first and second diffusion layers arranged in a semiconductor substrate to be adjacent to the first gate electrode; a first contact layer connected to the first diffusion layer of the first memory cell; a second contact layer connected to the first contact layer; a first bit line connected to the second contact layer and arranged above the first gate electrode of the first memory cell; a second memory cell having a second gate electrode, a third diffusion layer and a fourth diffusion layer, the third and fourth diffusion layers arranged in a semiconductor substrate to be adjacent to the second gate electrode, the second gate electrode of the second memory cell electrically connected to the first gate electrode of the first memory cell, the first and second memory cells arranged in a direction perpendicular to the first bit line; a second bit line connected to the third diffusion layer, arranged above the second gate electrode of the second memory cell, and arranged parallel to the first bit line; and a conductive layer commonly connected to the second

diffusion layer of the first memory cell and the fourth diffusion layer of the second memory cell, a height of the conductive layer substantially being coplanar with a height of the first contact layer.

Please amend the paragraph beginning at page 3, line 30, as follows:

A second aspect of the present invention is providing a semiconductor memory device ~~having a gate electrode and a diffusion layer, comprising a plurality of memory cells each of which including the gate electrode and the diffusion layer; an insulating film formed above side and top surfaces of the gate electrode of the semiconductor memory device; a first interlayer insulating layer formed between the gate electrode of the semiconductor memory device; a first contact layer formed in the first interlayer insulating layer and connected to the diffusion layer; a second interlayer insulting layer formed on the first inter layer insulating layer ; a second contact layer formed in the second interlayer insulating layer and connected to the first contact layer; a bit line connected to the second contact layer; and a conductive layer connected to at least two of the diffusion layers that are other than the diffusion layer connected to the first contact layer, at least two of the diffusion layers being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being the same as a height of the first contact layer~~, comprising: a plurality of memory cells each of which including a gate electrode and a diffusion layer; an insulating film formed above side and top surfaces of each gate electrode of the plurality of memory cells; a first interlayer insulating layer formed between two gate electrodes adjacent to each other; a first contact layer formed in the first interlayer insulating layer and connected to the diffusion layer; a second interlayer insulting layer formed on the first inter layer insulating layer ; a second contact layer formed in the second interlayer insulating layer and connected to the first contact layer;

a bit line connected to the second contact layer; and a conductive layer connected to at least two of the diffusion layers other than the diffusion layer connected to the first contact layer, the conductive layer formed between the two gate electrodes adjacent to each other being arranged in a direction vertical to the bit line, a height of the conductive layer substantially being coplanar with same as a height of the first contact layer.